REMARKS

Claims 1-3 and 5-7 are pending in the present application. Claims 4 and 8 are canceled above. Claim 1 is amended above.

Claims 4 and 8 are objected to for being of an improper format. Claims 4 and 8 are canceled above.

Claims 1-8 are rejected under 35 U.S.C 102(b) as being anticipated by the Manne publication. In view of the amendments and the following remarks, it is believed that the claims are allowable over Manne. Accordingly, reconsideration of the rejections is requested.

In the present invention as claimed, a multiplexer has a first input and a second input that receive a predicted conditional branch and an inverted predicted conditional branch, respectively. The multiplexer selects and outputs one of the predicted conditional branch and the inverted predicted conditional branch, based on a state of a single selection input of the multiplexer. In addition, in the present invention as claimed, a first state transition logic circuit generates accuracy history bits in response to the comparison signal generated by a comparator. The predicted accuracy history signal is a single most significant bit of the accuracy history bits and is directly applied to the single selection input of the multiplexer, wherein the single accuracy history signal selects between the predicted conditional branch and the inverted predicted conditional branch to be output as the final branch prediction outcome.

The features set forth in amended independent claim 1 are illustrated at least at Figure 2 of the present specification. In this example, a predicted conditional branch I(Sc) is generated by a pattern history table 25 and is provided directly to a first input of a multiplexer 70 and an inverted predicted conditional branch is provided directly to a second input of the multiplexer 70 (see Figure 2 of the present specification). The multiplexer 70 selects and outputs one of the predicted conditional branch and the inverted predicted conditional branch based on the state of an accuracy history signal I(Ac) provided as a single selection signal to the multiplexer 70. If the predicted accuracy history signal I(Ac) having a value of '1' is applied to the single selection control input of the multiplexer 70, the conditional branch prediction I(Sc) is output from the multiplexer 70 as a final branch prediction outcome present specification. If the predicted

conditional branch I(Sc) is not correct, the predicted accuracy history signal I(Ac) having a value of '0' is applied to the single selection input of the multiplexer 70, and the inverted conditional branch prediction is outputted from the multiplexer 70 as a final branch prediction outcome. In this manner, the branch predictor of the present invention can reduce misprediction more efficiently. In addition, a comparator 40 generates a comparison signal by comparing the predicted conditional branch I(Sc) with the real conditional branch Rc of the branch instruction. In this manner, the state transition logic circuit 50 receives the comparison signal and generates accuracy history bits in response to the comparison signal.

Hence, in accordance with the present invention, the multiplexer has a first input that receives a predicted conditional branch and a second input that receives an inverted predicted conditional branch. The multiplexer includes a single selection input which selects between the two inputs and outputs one of the predicted conditional branch and the inverted predicted conditional branch as a final branch prediction outcome. This is performed by the multiplexer in response to a predicted accuracy history signal which is applied to the single selection input to select one of the predicted conditional branch and the inverted predicted conditional branch. The accuracy history bits are generated by the first state transition logic circuit in response to the comparison signal, and stored to the accuracy history table, in response to the comparison signal. The predicted accuracy history signal is generated as a single bit, e.g., the most significant bit, of the accuracy history bits.

The Manne publication describes a family of conventional branch predictors that uses a Selective Branch Inversion (SBI) method as a confidence estimator to determine when the branch predictor is likely to be incorrect. In Manne, the SBI predictor comprises a conventional branch predictor, a prediction threshold, a confidence estimator, and an inversion threshold (see Manne, Figure 1). In addition, the SBI predictor comprises a three-input, one-output "select & invert" logic block (see Manne, Figure 6). For each branch prediction, the confidence estimator generates an output value that indicates whether the prediction is one of a "low-confidence" prediction or a "high confidence" prediction. During each branch prediction, a confidence counter (for example, a miss distance counter (MDC)) of the confidence estimator is compared

with the inversion threshold. If the confidence counter/MDC counter is less than the inversion threshold, the prediction is output as "low-confidence" indicating that the prediction is believed to be incorrect, whereby the branch prediction is inverted.

In addition, three predictions comprised of the output (b) of the branch predictor and two outputs (c0, c1) from two respective portions of a confidence estimator are combined using the "select & invert" logic block. The three inputs of the "select & invert" logic block receive the three predictions, respectively. The two outputs (c0, c1) of the confidence estimator are each outputted as either a predetermined high-confidence or low-confidence branch prediction. The output of the "select & invert" logic block is a combination of the three predictions, determined by a logic block equation: $\overline{(b*c0} + b*c1)$ (see Manne, Figure 6).

It is submitted that the Manne publication fails to teach or suggest the present invention set forth in the amended claims. Specifically, there is no teaching or suggestion in Manne that the "select & invert" logic block serves as a multiplexer that receives as a first input a predicted conditional branch and that receives as a second input an inverted predicted conditional branch, as claimed. Instead, as noted in the Office Action at page 5, lines 3-8, the branch prediction (b) is combined with the two confidence estimator predictions (c0,c1), in a manner such that when the three predictions are combined, an SBI prediction is outputted from the "select & invert" logic block. This logical combination of three logic signals performed by Manne is not the selection and output of one of two input signals performed by a multiplexer in response to a single selection input, as the applicant claims. That is, since the "select & invert" logic block of Manne combines the outputs of both the branch predictor and the two confidence estimator prediction signals as indicated by the aforementioned logic block equation, it follows that Manne fails to teach or suggest a multiplexer for selecting and outputting one of the predicted conditional branch and the inverted predicted conditional branch, as claimed. Moreover, since two inputs of the "select & invert" logic block of Manne receive the outputs (c0, c1) of the confidence estimator (referred to in the Office Action at page 4, section d as an "accuracy signal"), it follows that the "select & invert" logic block of Manne does not select and output one of the predicted conditional branch and the inverted predicted conditional branch based on a state

of a single selection input, as claimed. In other words, Manne performs logical operations on the branch prediction (b) using the two confidence estimation predictions (c0,c1) to combine the signals into an output prediction. In contrast, as set forth in the amended claims, the applicant's branch predictor uses a multiplexing approach in which one of the two inputs, namely, one of the predicted conditional branch and the inverted predicted conditional branch, is selected by a single selection signal, in the form of a single accuracy history bit. Thus, Manne fails to teach or suggest the applicant's claimed approach to selecting either a predicted conditional branch or an inverted predicted conditional branch based on a state of a single selection input of a multiplexer, as claimed.

Manne is cited in the Office Action at page 4-5, section 3, as disclosing a multiplexer that selects and outputs one of a number of inputs. However, the "select & invert" logic block in Manne does not select and output one of the three inputs, but instead combines the three inputs, such that an SBI prediction is outputted from the "select & invert " logic block from the combination of the three inputs, as determined by the logic block equation. Since the "select & invert" logic block combines the three inputs into a single output, it therefore follows that the "select & invert" logic block does not select and output one of the predicted conditional branch and the inverted predicted conditional branch in response to a single selection signal, as now set forth in the amended claims.

In addition, Manne performs a comparison between the miss distance counter (MDC) and the inversion threshold to determine whether a branch is correctly predicted. In response to this comparison, Manne teaches that the low confidence and high confidence branch predictions are generated and outputted to the "select and invert" logic block. In contrast, as set forth in the amended claims, and as described above, the applicant's branch predictor teaches a first state transition logic circuit that receives a comparison signal from a comparator. In response to the comparison signal, the first state transition logic circuit generates the accuracy history bits. The predicted accuracy history signal is a single most significant bit of the accuracy history bits and is directly applied to the single selection input of the multiplexer. The applicant's branch predictor performs no comparison as disclosed in Manne between a miss distance counter (MDC) and an

inversion threshold that results in a high confidence branch prediction or a low confidence branch prediction. Instead, the applicant teaches a comparison performed by the comparator that compares the predicted conditional branch with a real conditional branch, and generates the resulting comparison signal. Thus, it follows that Manne fails to teach or suggest the applicant's invention with regard to generating a predicted accuracy history signal.

For at least these reasons, it is submitted that Manne fails to teach or suggest the invention set forth in the amended claims. Therefore, reconsideration of the rejection of claims 1-8 under 35 U.S.C. 102(b) based on Manne is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Steven M. Mills
Registration Number 36,610
Attorney for Applicants

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0162\amendb\amendmentb2.wpd